

## MM74HC240 Inverting Octal 3-STATE Buffer

### General Description

The MM74HC240 3-STATE buffer utilizes advanced silicon-gate CMOS technology. It possesses high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. It has a fanout of 15 LS-TTL equivalent inputs.

The MM74HC240 is an inverting buffer and has two active LOW enables ( $\overline{1G}$  and  $\overline{2G}$ ). Each enable independently controls 4 buffers.

All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

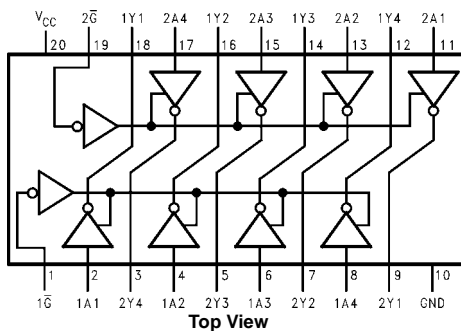
- Typical propagation delay: 12 ns
- 3-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80  $\mu$ A (74 Series)
- Output current: 6 mA

### Ordering Code:

Order Number	Package Number	Package Description
MM74HC240WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC240N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

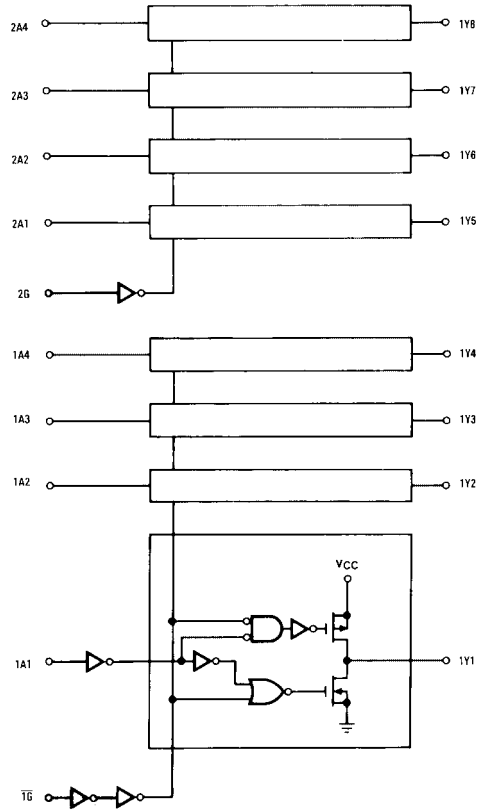


### Truth Table

$\overline{1G}$	1A	1Y	$\overline{2G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = HIGH Level  
L = LOW Level  
Z = HIGH Impedance

Logic Diagram



**Absolute Maximum Ratings** (Note 1)

(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}+1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}+0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 35$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 70$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ ) $V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: — 12 mW/°C from 65°C to 85°C.

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				Typ	Guaranteed Limits			
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0$ mA $ I_{OUT}  \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0$ mA $ I_{OUT}  \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$
$I_{OZ}$	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND $\bar{G} = V_{IH}, G = V_{IL}$	6.0V		$\pm 0.5$	$\pm 5$	$\pm 10$	$\mu A$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$

**Note 4:** For a power supply of 5V  $\pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

## AC Electrical Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $t_r = t_f = 6$  ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay	$C_L = 45$ pF	12	18	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Enable Delay to Active Output	$R_L = 1$ k $\Omega$ $C_L = 45$ pF	14	28	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Disable Delay from Active Output	$R_L = 1$ k $\Omega$ $C_L = 5$ pF	13	25	ns

## AC Electrical Characteristics

$V_{CC} = 2.0V$  to  $6.0V$ ,  $C_L = 50$  pF,  $t_r = t_f = 6$  ns (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay	$C_L = 50$ pF	2.0V	55	100	126	149	ns
		$C_L = 150$ pF	2.0V	80	150	190	224	ns
		$C_L = 50$ pF	4.5V	12	20	25	30	ns
		$C_L = 150$ pF	4.5V	22	30	38	45	ns
		$C_L = 50$ pF	6.0V	11	17	21	25	ns
$t_{PZH}$ , $t_{PZL}$	Maximum Output Enable Time	$R_L = 1$ k $\Omega$						
		$C_L = 50$ pF	2.0V	75	150	189	224	ns
		$C_L = 150$ pF	2.0V	100	200	252	298	ns
		$C_L = 50$ pF	4.5V	15	30	38	45	ns
		$C_L = 150$ pF	4.5V	20	40	50	60	ns
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time	$R_L = 1$ k $\Omega$	2.0V	75	150	189	224	ns
		$C_L = 50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per buffer) $\bar{G} = V_{IH}$ $\bar{G} = V_{IL}$		12 50				pF pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF
$C_{OUT}$	Maximum Output Capacitance			10	20	20	20	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

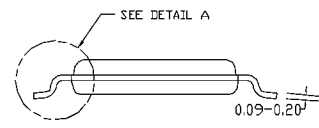
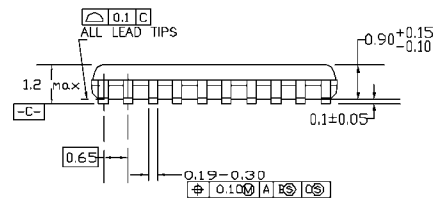
**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

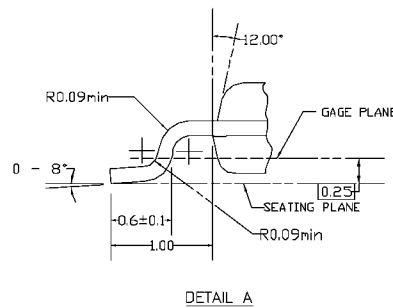


PIN #1 IDENT.

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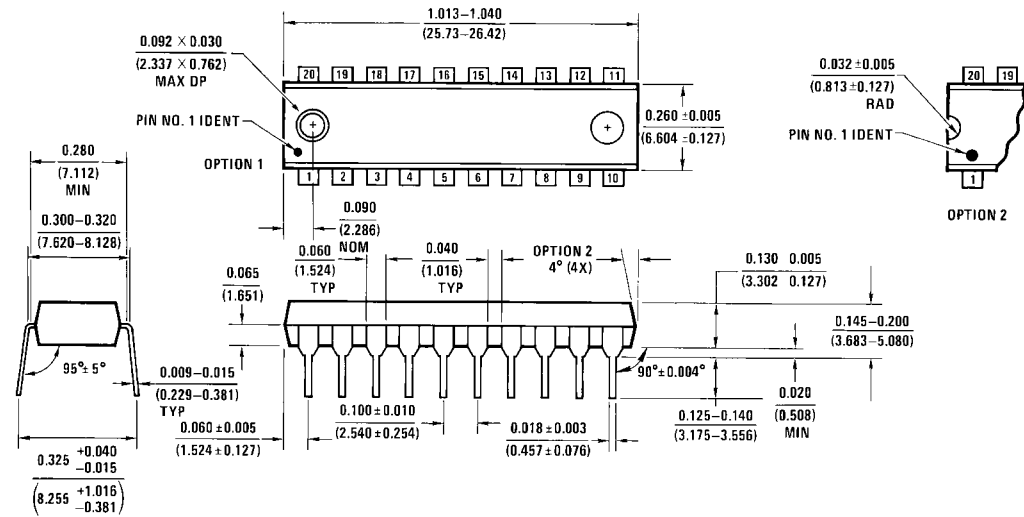


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

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